What is claimed is:

1. A charge transfer device having a charge transfer portion in which a plurality of electrode pairs are formed above a transfer channel, comprising:

means for commonly wiring said plurality of electrode pairs forming N (N=2, 3, 4, ··· natural numbers) bits of said charge transfer portion so that electrode pairs of each half bit can be independently driven at every N bits;

means for, in a normal operation, inputting said electrode pairs of each half bit with the same drive pulse to operate it by a two-phase complementary drive; and

means for, in an N-time speed operation, inputting said electrode pairs of N bits with N pairs of complementary drive pulses to operate them by a 2N-phase complementary drive.

2. A charge transfer device according to claim 1, wherein a phase of a drive pulse applied to said electrode pair at the last stage of said charge transfer portion is the same as a phase of one of two phases of a drive pulse in said normal operation.

3. A charge transfer device according to claim 1, wherein said charge transfer portion is a horizontal transfer portion, a read out gate between vertical charge transfer portions corresponding to respective light receiving portion columns can be driven at one to N columns, in said normal

operation all of said read out gates are set on to read a signal, and in said N-time speed operation only one of said N-column read out gates is set on to read a signal of 1/N columns.

4. A charge transfer device according to claim 1, further comprising:

a drain region provided under said horizontal charge transfer portion for draining charges through a gate portion, wherein in said N-time speed operation said gate portion is set on during a horizontal blanking period, signal charges corresponding to (N-1) columns of N columns of light receiving portions are drained to said drain region and then charges are transferred by said horizontal charge transfer portion.

5. A method of driving a charge transfer device having a charge transfer portion in which a plurality of electrode pairs are formed above a transfer channel and arranged such that said plurality of electrode pairs forming N (N=2, 3, 4, ··· natural numbers) bits of said charge transfer portion are wired at every so that electrode pairs of each half bit can be independently driven at every N bits, comprising the steps of:

in a normal operation, inputting said electrode pairs of each half bit with the same drive pulse to operate it by a two-phase complementary drive; and

in an N-time speed operation, inputting said electrode pairs of N bits with N pairs of complementary drive pulses to operate them by a 2N-phase complementary drive.

6. A driving method according to claim 5, wherein a phase of a drive pulse applied to said electrode pair at the last stage of said charge transfer portion is the same as a phase of one of two phases of a drive pulse in said normal operation.

7. A driving method according to claim 5, wherein said charge transfer portion is a horizontal transfer portion, a read out gate between vertical charge transfer portions corresponding to respective light receiving portion columns can be driven at one to N columns, in said normal operation all of said read out gates are set on to read a signal, and in said N-time speed operation only one of said N-column read out gates is set on to read a signal of 1/N columns.

8. A driving method according to claim 5, wherein a drain region is provided under said horizontal charge transfer portion for draining charges through a gate portion, and wherein in said N-time speed operation said gate portion is set on during a horizontal blanking period, signal charges corresponding to (N-1) columns of N columns of light receiving portions are drained to said drain region and then charges are transferred by said horizontal charge transfer portion.

9. A charge transfer device, comprising:

an electrode structure formed of electrode pairs for

first and second phases repeatedly and alternately arranged above a transfer channel in its transfer direction and wired such that said electrode pairs for the first phase located across said electrode pairs for the second phase can be independently driven;

means for applying a DC voltage to said electrode pairs for the second phase; and

means for supplying transfer clocks having a phase reverse each other to each of said electrode pairs for the first phase located across each of said electrode pairs for the second phase.

10. A solid-state imaging device comprising:

an imaging unit formed of a plurality of pixels for converting an incident light into a signal charge; and

a charge transfer portion for transferring signal charges read out from said plurality of pixels, wherein said charge transfer portion has an electrode structure formed of electrode pairs for first and second phases repeatedly and alternately arranged above a transfer channel in its transfer direction and wired such that said electrode pairs for the first phase located across said electrode pairs for the second phase can be independently driven, a mode setting unit for setting an operation mode, and means for, when said mode setting unit sets a first operation mode, supplying a DC voltage or a transfer clock having a phase reverse to that of the transfer clock for the first phase to the electrode pair for the second phase and

supplying a transfer clock having the same phase as that of the transfer clock to each of said electrode pairs located across said electrode pair for the second phase and for, when said mode setting unit sets a second operation mode, applying a DC voltage to said electrode pair for the second phase and supplying transfer clocks having reverse phase to each of said electrode pairs for the first phase located across said electrode pair for the second phase.

11. A solid-state imaging device according to claim 10, wherein said charge transfer portion carries out a transfer operation in said first operation mode with employing an mount of one pixel as one cycle and carries out a transfer operation in said second operation mode with employing an amount of two pixels as one cycle.

12. A solid-state imaging device according to claim 11, wherein in said second operation mode a phase of a transfer clock at a final stage is the same as a phase of the transfer clock at the final stage in said first operation mode.

13. A solid-state imaging device according to claim 10, wherein in said second operation mode a signal charge is selectively transferred at every predetermined repeated pixel of said plurality of pixels in the transfer direction.

14. A solid-state imaging device according to claim

13, wherein said imaging unit comprises a plurality of pixels arranged in a matrix fashion, a plurality of vertical transfer portions each of which is provided at every vertical column of said plurality of pixels, and a read out gate portion for, in said first operation mode, reading signal charges out from all of said plurality of pixels to said vertical transfer portions and for, in said second operation mode, selectively reading signal charges out from respective predetermined repeated pixels of said plurality of pixels in the transfer direction to said vertical transfer portions.

15. A solid-state imaging device according to claim 13, wherein said imaging unit comprises a plurality of pixels arranged in a matrix fashion, a plurality of vertical transfer portions each of which is provided at every a vertical column of said plurality of pixels and which vertically transfers a signal charge read out from each of said plurality of pixels, and a control gate portion for selectively transferring a signal charge of each of predetermined repeated pixels in the horizontal direction of said plurality of pixels to said charge transfer portion from said plurality of vertical transfer portions.

16. A solid-state imaging device according to claim 13, wherein said charge transfer portion comprises a charge draining portion for draining a signal charge other than signal charges of the predetermined repeated pixels in the transfer

direction of signal charges of said plurality of pixels transferred from said imaging unit.

17. A method of driving a solid-state imaging device which has an imaging unit formed of a plurality of pixels for converting an incident light into a signal charge, and a charge transfer portion for transferring signal charges read out from said plurality of pixels and in which said charge transfer portion has an electrode structure formed of electrode pairs for first and second phases repeatedly and alternately arranged above a transfer channel in its transfer direction and wired such that said electrode pairs for the first phase located across said electrode pairs for the second phase can be independently driven, comprising the steps of:

in a first operation mode, supplying a DC voltage or a transfer clock having a phase reverse to that of a transfer clock for the electrode pairs for the first phase to the electrode pairs for the second phase and supplying a transfer clock having the same phase to each of said electrode pairs for the first phase located across said electrode pair for the second phase; and

a second operation mode, applying a DC voltage to said electrode pairs for the second phase and supplying transfer clocks having reverse phase to each of said electrode pairs for the first phase located across said electrode pair for the second phase.

18. A driving method according to claim 17, wherein said charge transfer portion carries out a transfer operation in said first operation mode with employing an mount of one pixel as one cycle and carries out a transfer operation in said second operation mode with employing an amount of two pixels as one cycle.

19. A driving method according to claim 17, wherein in said second operation mode a phase of a transfer clock at a final stage is the same as a phase of the transfer clock at the final stage in said first operation mode.

20. A driving method according to claim 17, wherein in said second operation mode a signal charge is selectively transferred at every predetermined repeated pixel of said plurality of pixels in the transfer direction.

21. A driving method according to claim 20, wherein said imaging unit comprises a plurality of pixels arranged in a matrix fashion, a plurality of vertical transfer portions located at each of vertical columns of said plurality of pixels and read out gate portions provided between each of vertical columns of said plurality of pixels and each of corresponding vertical transfer portions, and wherein in said first operation mode, signal charges are read out from all of said plurality of pixels to said vertical transfer portions by using said read out gate, and in said second operation mode, signal charges are

selectively read out from respective predetermined repeated pixels of said plurality of pixels in the transfer direction to said vertical transfer portions by using said read out gate.

22. A driving method according to claim 20, wherein said imaging unit comprises a plurality of pixels arranged in a matrix fashion, a plurality of vertical transfer portions each of which is provided at each of a vertical columns of said plurality of pixels and which vertically transfers a signal charge read out from each of said plurality of pixels, and a control gate portion located between said imaging unit and said charge transfer portion, wherein said control gate portion selectively transfers a signal charge of each of predetermined repeated pixels in the horizontal direction of said plurality of pixels to said charge transfer portion from said plurality of vertical transfer portions.

23. A driving method according to claim 20, wherein said charge transfer portion comprises a charge draining portion for draining a signal charge which drains signal charges other than signal charges of the predetermined repeated pixels in the transfer direction of signal charges of said plurality of pixels transferred from said imaging device.